

A 1.9-GHz GaAs Chip Set for the Personal Handyphone System

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The Japanese Personal Handyphone System (PHS) is representative of the latest generation of digital portable communications systems currently being deployed. Enabling technologies for these systems include high performance Radio Frequency Integrated Circuit (RFIC) chip sets. These chip sets allow all the RF transceiver functions to be included in low cost surface mount plastic packages. With the addition of filters and bypassing capacitors, the RF portion of the phone shares the same printed circuit board (PCB) as the DSP, CODEC, and Logic IC's. The availability of such highly integrated 1.9-GHz RFIC's requires the solution of many complex design, manufacturing, and test problems. This paper explains the critical issues relating to the air interface of the PHS system and how it affects the RFIC design. The chip partition, design, and performance of each subfunction is discussed relative to the requirements imposed by the air interface. The result is a highly integrated, cost effective solution that occupies the minimum board area.

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